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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	09/964,586	FRUTSCHY ET AL.	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,3,7-9,65-76,78,79,84,85,89,91 and 92* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7,9,65-76,78,79,84,85,89,91 and 92* is/are rejected.

7)☒ Claim(s) *2,3 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9-21-01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 7, 9, 65-75, 78 and 84 are rejected under 35 U.S.C. 102(e) as being anticipated by Dibene, II et al. (US Pat. 6452113).

Regarding claims 78 and 84, Dibene, II et al. disclose a power module (see 600 in Fig. 6A/6B) having integrated circuits (IC)/an IC package comprising:

- a substrate (702 of an assembly 700 in Fig. 9 and 7) supporting the microprocessor/IC die (310 in Fig. 7; Col. 8, line 66) on the IC die of the substrate
- the power module (600/602 in Fig. 6A-9) comprising a packaged circuit board (PCB)/package frame (602 in Fig. 6A/6B and 9; Col. 8) mounted/attached directly at a peripheral area and above a perimeter of the substrate and not upon an interposer (see Fig. 9 and Fig. 7; Col. 4, lines 25-28; Col. 8, lines 60-68; Col. 9,

line 25) and arranged on the die- side of the substrate apart from the IC die on the substrate, and

- the power module providing a low impedance, low inductance power/current path directly to the die (see 608A/608B and 612A/612B respectively in Fig. 6A/6B) and not via the interposer, and being functional as a power/ground impedance deliverer (PGID) to provide power/ground impedance delivery path/circuit (Col. 7, line 53- Col. 9, line 37)

(Fig. 6A-12; Col. 7, line 50- Col 10, line 25).

Dibene, II et al. further teach:

- the electrical connections/structure being functional as a mechanical support/stiffener as well as the PGID, the dual functions including mechanical functions comprising conductive interconnects providing a coupling/rigidity/support for the substrate (Col. 8, lines 50-60) and mechanical fasteners (802 in Fig. 9) proving the predetermined level of mechanical fastening/stiffening (Col. 9, lines 32-37), and
- a variety of module assembly configurations including an embodiment where the package frame (see 2204 in Fig. 22) is positioned/mounted/attached at a peripheral/corner area including a perimeter of the substrate and extends along the perimeter and two side edges of the substrate (see 2204 and 2202 in Fig. 22; Fig. 22-25; Col. 14, line 16- Col. 15, line 22).

Regarding claim 7, Dibene II, et al. teach the entire claimed structure as applied to the claim 78 above, wherein Dibene II et al. further teach the PCB/package frame being made of an electrically conducive surfaces/sections using conventional circuit board fabrication processing including etching and metallization (Col. 8, lines 24-37) to withstand conditions/temperature of normal IC operation (Col. 3, 4 and 7-16)

Regarding claim 7, making or depositing the frame do not distinguish over Dibene II et al., regardless of the process for forming the frame, because only the final product is relevant, not the process of making such as "molding/stamping/etching, etc. or laminating ". Note that a "produced by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685., In re Luck, 177 USPQ 523., In re Fessmann, 180 USPQ 324., In re Avery, 186 USPQ 161', In re Wedheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issuel; and In re Marrosi et al., 218 USPQ 289, all of which make it clear that it is the patentability and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not . Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 706.03(e).

Regarding claim 9, Dibene II, et al. teach the entire claimed structure as applied to the claim 78 above, wherein Dibene II et al. further teach a heat sink/heat

spreader plate assembly (1006/1010/1004 in Fig. 10-11B) being bonded to/supported on the PCB/package frame (Col. 9, line 40-67).

Regarding claims 65-69, Dibene II, et al. teach the entire claimed structure as applied to the claim 84 above, wherein Dibene II et al. further teach:

- the package frame being configured to be functional as the PGID for the module and being in a form of a ring having a central aperture (604 in Fig. 6A/6B; Col. 8, line 26)

- the package frame/PGID comprising two separate components/sections (see 1402 and 1404 in Fig. 14) being positioned on the respective section of the substrate (Col. 10, lines 35- Col. 11), the corner edges of the sections having rounded corners, and

- the package frame/PGID comprising two separate components/sections including corner edges (see 1402 and 1404 in Fig. 14) being positioned on the respective section of the substrate (Col. 10, lines 35- Col. 11), the comer edges having rounded corners.

Regarding claim 70, Dibene II, et al. teach the entire claimed structure as applied to the claim 84 above, wherein Dibene II et al. teach the package frame/PGID and the substrate being made of conventional circuit board material comprising insulating material/portions and metallized components/circuit layers (Col. 8, line 6, Col.

9, line 10), the package frame/PGID and the substrate having similar thermal properties such as coefficient of thermal expansion (CTE).

Regarding claims 71-73, Dibene, II et al. teach the entire claimed structure as applied to claim 84 above, except the PGID having a ground side and power side portions and having insulating couplers separating the power and ground portions and providing an aid in the structural integrity of the PGID.

Dibene, II et al. further teach the package frame/PGID comprising:
- plated through-holes and electrically conductive surfaces/pads (610, 616A/B respectively in Fig. 6A/B, Col. 8, lines 25-50) being electrically connected to a conductive interconnect spacer having electrically conductive portions (612A/612B in Fig. 6A), the conductive layer/plating being copper (Cu)
- the conductive interconnect spacer providing dual functions including a mechanical support/coupling with the substrate and two separate conductive paths (616A and 616B in Fig. 6A/6B) including a first power path and a second ground path respectively in a coaxial arrangement (Col. 8, lines 50-68), and
- the electrically conductive portions of the conductive interconnect spacer being separated by an insulating dielectric portion/coupling section (612 C in Fig. 6A; Col. 8, lines 37-47).

Dibene, II et al. further teach in embodiments of Fig. 13 and 14, the PGID configuration comprising power and ground conductive paths being provided in two concentric metal rings electrically isolated from each other (see 1306/1304 and 1404/1402 respectively in Fig. 13 and 14, Col. 10, lines 35- Col. 11, line 15) and being bonded/soldered to provide an integral structure providing the desired power/ground paths from the die to the substrate.

Regarding claims 74 and 75, Dibene II, et al. teach the entire claimed structure as applied to the claim 84 above, wherein Dibene II et al., further teach a heat sink/heat spreader plate/assembly (1006/1010/1004 in Fig. 10-1 1B) being integrally bonded to/coupled/supported on the package frame/PGID (Col. 9, line 40-67) such that the package frame/PGID and the IC die are in between the spreader plate and the substrate (see 602, 1006/1004, 302 and 702 respectively in Fig. 6A-11B).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 76 and 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dibene, II et al. (US Pat. 6452113) in view of Belady (US Pat. 6285550).

Regarding claims 76 and 89, Dibene II, et al. teach substantially the entire claimed structure as applied to claims except a plurality of power pods/power pod supplying the power to the IC die.

It is conventional in chip packaging and power supply/interconnect technology art to one or more power supply sources or power pods connecting various connectors and components in a power module. Belady teaches a power module having a variety of electrical components including a substrate, microprocessor/die, heat sink, etc. where power supply is arranged through a conventional power pod (Col. 9, lines 17-23, Col. 8-10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the plurality of power pods supplying the power to the IC die as taught by Belady so that the desired flexibility in power supply arrangement can be achieved and the reliability of the power supply can be improved in Dibene, II et al's package.

5. Claims 79, 85 and 92 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dibene, II et al. (US Pat. 6452113) in view of Hembree et al. (US Pat. US Pat. App. Pub. 2001/0001542).

Regarding claims 79, 85 and 92, Dibene II, et al. teach substantially the entire claimed structure as applied to the claims 76, 78 and 84 above, except the stiffener/package frame including a capacitor or a capacitor including an insulator.

Hembree et al. teach a power supply delivery carrier/system comprising a variety of configurations including capacitors (see 38, 38A, etc. in Fig. 4-4E

and 12) having electrodes connected to the desired power/ground path in a base substrate or an

interconnect of the system/carrier, the capacitor inherently including an insulator (sections 0010-0057, 0089-0098).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the capacitor or the capacitor including an insulator as taught by Hembree et al. so that the electrical performance can be improved and the desired electrical routing can be achieved in Dibene, II et al's package.

6. Claim 91 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dibene, II et al. (US Pat. 6452113) and Belady (US Pat. 6285550) as applied to claim 76 above, and further in view of Hembree et al. (US Pat. US Pat. App. Pub. 2001/0001542).

Regarding claim 91, Dibene II, et al., Belady and Hembree et al. teach substantially the entire claimed structure as applied to the claims 76, 78 and 79 above.

Allowable Subject Matter

7. Claims 2, 3 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to the rejected claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

6-19-06

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800